## **CLAIMS**

## What is claimed is:

- 1. An apparatus, comprising:
  - a semiconductor die having a through via formed therein;
- a first interconnect formed on a frontside of the die and a second interconnect formed on a backside of the die coupled with the through via; and
- a first package substrate electrically coupled with the first interconnect and a second package substrate electrically coupled with the second interconnect.
- 2. The apparatus of claim 1, further comprising a first underfill layer between the front side of the die and the first substrate and a second underfill layer between the backside of the die and the second substrate.
- 3. The apparatus of claim 1, further comprising a substrate ball electrically coupled between the first and second substrates.
- 4. The apparatus of claim 1, wherein the first and second interconnects comprise solder balls.
- 5. The apparatus of claim 1, wherein the semiconductor die is thinned using one selected from the group consisting of a backgrinding process, a chemical mechanical polishing (CMP) process, and a spin etching process.

- 6. The apparatus of claim 2, wherein the underfill layers comprise a no-flow underfill material.
- 7. The apparatus of claim 1, wherein the front side of the die comprises an active side of the die.
- 8. The apparatus of claim 1, wherein the substrates are package substrates to distribute signals to and from the semiconductor die.
- 9. The apparatus of claim 8, wherein signals comprise an input/output (IO) signal and a power signal.
- 10. A method, comprising:

forming a through via in a back side of a semiconductor die and attaching a first interconnect to the through via;

attaching a second interconnect to a device side of the die; electrically coupling the first interconnect to a first substrate; and electrically coupling the second interconnect to a second substrate.

- 11. The method of claim 10, wherein the through via connects with the device side.
- 12. The method of claim 10, further comprising:dispensing a first underfill layer on the first package substrate; anddispensing a second underfill layer on the backside of the semiconductor die.

- 13. The method of claim 12, further comprising:
  attaching a substrate ball between the first and second package substrates.
- 14. The method of claim 10, wherein the first and second interconnects comprise solder balls.
- 15. The method of claim 10, further comprising thinning the semiconductor die.
- 16. The method of claim 10, wherein the first and second underfill layers comprise a no-flow underfill.
- 17. The method of claim 10, wherein the first and second substrates comprise a first and second package substrate to distribute signals to the semiconductor die.
- 18. An apparatus, comprising:

a semiconductor die having a through via formed in a backside of the die, the through via to provide a path to a device side of the die;

a first solder ball coupled with the through via, and a second solder ball coupled with the device side;

a first package substrate electrically coupled with the first solder ball to distribute signals to the through via and the back side of the die;

a second package substrate electrically coupled with the second solder ball to distribute signals to the device side of the die.

- 19. The apparatus of claim 18, wherein the semiconductor die is thinned to form the through via.
- 20. The apparatus of claim 18, wherein the first and second solder ball are controlled collapse chip connection (C4) attachments.
- 21. The apparatus of claim 18, further comprising a substrate ball to electrically couple the first and second package substrates.